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10/631,939	07/31/2003	Gerard Chauvel	TI-35710 (1962-05423)	9644

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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
08/17/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/631,939	CHAUVEL ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-7,10,11,14,17 and 20-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,10,11,14,17 and 20-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/26/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 5-7, 10-11, 14, 17, and 20-24 are pending.

2. The office acknowledges the following papers:

Claims, IDS, and arguments filed 7/13/2007.

Maintained Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 5-7, 10-11, 14, 17, 20-21, and 23 are rejected under 35 U.S.C. §103(a) as being unpatentable over Feierbach et al. (U.S. 6,088,786), in view of Seal et al. (U.S. 6,965,984), in view of Kloth (U.S. 6,549,961).

5. As per claim 1:

Feierbach disclosed a system, comprising:

A first processor (Feierbach: Figure 2 element 204, column 6 lines 53-67 continued to column 7 lines 1-7);

A second processor coupled to the first processor, the second processor having a core and comprising stack storage residing in the core (Feierbach: Figure 2 elements 104 and 210, column 6 lines 53-67 continued to column 7 lines 1-7);

Memory coupled to, and shared by, the first and second processors (Feierbach: Figure 2 element 212, column 6 lines 53-65)(The data cache is shared by the two

processors.); and

A synchronization unit coupled to the first and second processors, said synchronization unit synchronizes the execution of the first and second processors (Feierbach: Figure 4 element 402, column 10 lines 25-55)(The copy unit monitors data accesses and ensures that data is properly exchanged between processors and other memory units. Thus having the same functionality.);

Wherein the second processor executes stack-based instructions (Feierbach: Figure 2 element 202, column 6 lines 53-65) while the first processor executes one or more tasks (Feierbach: Column 6 lines 21-29)(Feierbach incorporates by reference Yung (U.S. 5,996,066))(Yung: Figure 1, column 3 lines 20-67) wherein the first processor manages the memory via an operating system that executes only on the first processor (Feierbach: Column 6 lines 21-29)(Feierbach incorporates by reference Yung (U.S. 5,996,066))(Yung: Figure 1 elements 44a-b, column 3 lines 20-67)(Yung manages memory through the hardware memory management units. An operating system manages memory through software. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that the processor of Yung could have managed memory from software using an operating system instead of hardware using the memory management units.) and the second processor executes a virtual machine that controls the execution of a program on the second processor (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 1 element 100, column 5 lines 35-54)(The stack processor runs a virtual machine that controls the execution of instructions.).

Feierbach failed to teach the first processor executes a virtual machine that controls the execution of a program on the second processor; wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode; and wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor.

However, Seal disclosed the first processor executes a virtual machine that controls the execution of a program on the second processor (Seal: Figure 18 element 326, column 16 lines 38-48; Figure 20, column 17 lines 38-67)(The processor includes a virtual machine to execute Java bytecodes. Some of the instructions can't be run on the processor, and are executed by software. Thus having the same functionality.).

An advantage of having the first processor process Java bytecodes through acceleration techniques is that the instructions will run faster on the hardware as opposed to the software executing the instructions (Seal: Column 1 lines 19-47). The instructions that are too complex to be executed on hardware are sent off to be executed on software (Seal: Column 1 lines 19-47). One of ordinary skill in the art would have been motivated to use a virtual machine to assist in accelerating Java bytecode instructions for the benefit of increased performance from the accelerated instructions being executed in hardware. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to add a virtual machine to help

accelerate Java bytecodes for the advantage of increased performance.

Feierbach and Seal failed to teach wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode *and* wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor.

However, Kloth disclosed wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode (Kloth: Figure 2 elements 42, 44, and 48, column 3 lines 51-67 continued to column 4 lines 1-15)(When the first processor requests an unavailable resource, the processor suspends all execution while the halt signal is asserted. This causes the first processor accessing the unavailable resource to have reduced performance from stalling execution.).

Wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor (Kloth: Figure 3 elements 60, 62, 66, and 68, column 4 lines 16-32)(The second processor that is using the protected resource sends a release signal to the first processor being stalled. Figure 1, element 24 acts as the synchronization unit that stores the semaphores for the processors.).

The advantage of using semaphores is that they are able to resolve resource

conflicts between processors (Kloth: Column 1 lines 20-30). One of ordinary skill in the art would have been motivated by this advantage to implement semaphores in the processor of Feierbach and Seal. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement semaphores for the advantage of resolving resource conflicts.

6. As per claim 2:

Feierbach, Seal, and Kloth disclosed the system of claim 1 wherein the second processor comprises an internal data memory that holds a contiguous block of memory defined by an address stored in a register, and wherein local variables are stored in said data memory (Feierbach: Column 6 lines 13-21)(Feierbach incorporates by reference Tremblay et al. (U.S. 6,021,469))(Tremblay: Figure 4a-b, columns 9-11).

7. As per claim 5:

Feierbach, Seal, and Kloth disclosed the system of claim 1 wherein the stack-based instructions comprise Java bytecodes (Feierbach: Column 5 lines 4-29) and the first processor comprises a RISC processor (Seal: Figure 10 element 12, column 5 lines 60-67 continued to column 6 lines 1-9) so that the RISC processor executes one or more tasks while the second processor executes Java code.

8. As per claim 6:

Feierbach, Seal, and Kloth disclosed the system of claim 1 further including a main stack residing outside the second processor's core and coupled to the stack storage in the second processor's core (Feierbach: Figure 2 element 212, column 7 lines 8-18).

9. As per claim 7:

Feierbach, Seal, and Kloth disclosed the system of claim 6 wherein the stack storage in the second processor's core provides an operand to execute a stack-based instruction in the second processor (Feierbach: Figure 2 element 210, column 7 lines 50-65).

10. As per claim 10:

Claim 10 essentially recites the same limitations of claim 1. Therefore, claim 10 is rejected for the same reasons as claim 1.

11. As per claim 11:

Claim 11 essentially recites the same limitations of claim 2. Therefore, claim 11 is rejected for the same reasons as claim 2.

12. As per claim 14:

Claim 14 essentially recites the same limitations of claims 6-7. Therefore, claim 14 is rejected for the same reasons as claims 6-7.

13. As per claims 17:

Claim 17 essentially recites the same limitations of claim 1-2. Therefore, claim 17 is rejected for the same reasons as claim 1-2.

14. As per claim 20:

Feierbach, Seal, and Kloth disclosed the system of claim 1 wherein a clock internal to the first processor is disabled thereby effectuating the reduced power or reduced performance mode (Kloth: Figure 2 element 48, column 4 lines 3-15)(When the first processor requests an unavailable resource, the processor suspends all execution

while the halt signal is asserted. This causes the first processor accessing the unavailable resource to reduce performance from stalling execution. Official notice is given that while the processor is in a wait state, the clock could be gated with the wait signal to disable the clock which results in a reduced power mode.).

15. As per claim 21:

Feierbach, Seal, and Kloth disclosed the system of claim 1 wherein said wait signal remains asserted until said synchronization unit deasserts said wait signal (Kloth: Figure 3 element 68, column 4 lines 16-32)(The second processor that is using the protected resource sends a release signal to the first processor being stalled. Figure 1, element 24 acts as the synchronization unit that stores the semaphores for the processors).

16. As per claim 23:

Feierbach, Seal, and Kloth disclosed the system of claim 17 wherein said synchronization unit continues to assert said first signal until either the synchronization unit receives said second signal from the second processor or the synchronization unit receives an interrupt signal (Kloth: Figure 3 element 68, column 4 lines 16-32)(The second processor that is using the protected resource sends a release signal to the first processor being stalled. Figure 1, element 24 acts as the synchronization unit that stores the semaphores for the processors).

17. Claims 22 and 24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Feierbach et al. (U.S. 6,088,786), in view of Seal et al. (U.S. 6,965,984), in view of Kloth (U.S. 6,549,961), further in view of Evoy et al. (U.S. 5,951,689).

18. As per claim 22:

Feierbach, Seal, and Kloth disclosed the system of claim 1.

Feierbach, Seal, and Kloth failed to teach wherein said second processor asserts said wait release signal when said second processor requires support from said first processor.

However, Evoy disclosed wherein said second processor asserts said wait release signal when said second processor requires support from said first processor (Evoy: Figure 1 element 39, column 3 lines 29-36 and lines 60-67 continued to column 4 lines 1-7)(Element 39 allows for the processor functional units to be in high or low performance mode. Element 39 is in high performance mode when extra functional units are needed to deliver higher performance for an application. It would have been obvious to one of ordinary skill in the art at the time of the invention that this could also be applied to a multiprocessor system in order to turn on and off processors when they are needed and when they aren't needed.).

The advantage of a power control system is that it will allow for slower performance and power savings when an application isn't in need of high performance (Evoy: Column 1 lines 35-49). One of ordinary skill in the art would have been motivated by this advantage to implement power control for the multiprocessor system of Kloth to enable processors to be shut off to save power when they weren't needed.

Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a power control unit to regulate which processors are turned on and which are turned off for the advantage of power savings when processors aren't needed.

19. As per claim 24:

The additional limitation(s) of claim 24 essentially recite the additional limitation(s) of claim 22. Therefore, claim 24 is rejected for the same reason(s) as claim 22.

Response to Arguments

20. The arguments presented by Applicant in the response, received on 7/13/2007 are not considered persuasive.

21. Applicant argues that "Kloth failed to teach wherein the first processor executes a transaction targeting a pre-determined address and the synchronization unit detects said pre-determined address and asserts a wait signal to cause said first processor to enter a reduced power or reduced performance mode" for claims 1, 10, and 17.

This argument is not found to be persuasive for the following reason. Applicant additionally states that Kloth disclosed a system where if the requested resource is available, then a halt signal is not asserted. The examiner agrees that this is shown in figure 2 element 46, but states that this was not cited as reading upon the claimed limitation. Instead, elements 42, 44, and 48 of figure 2 were cited as reading on the claimed limitation. These elements states that a first processor attempts to access data

at a certain address, and checks to see if the resource is currently protected. Element 48 states that the resource is currently protected and tells the first processor to suspend all execution while the halt signal is asserted (Kloth: Column 4 lines 4-6). The halting of the processor causes the performance of the processor to be reduced. Thus, Kloth correctly reads upon the claimed limitation.

22. Applicant argues that "Kloth failed to teach wherein said second processor asserts a wait release signal that is received by said synchronization unit and that causes said synchronization unit to deassert said wait signal to the first processor" for claims 1, 10, and 17.

This argument is not found to be persuasive for the following reason. Applicant additionally states that Kloth disclosed a system where if another processor is not waiting to access the released resource then the halt signal is not deasserted. The examiner agrees that this is shown in figure 3 element 64, but states that this was not cited as reading upon the claimed limitation. Instead elements 60, 62, 66, and 68 are cited as reading on the claimed limitation. These elements state that there is another processor waiting for the resource to be released by a second processor. Element 68 states that a halt release signal is sent to the waiting processor to alert it that it can now access the formerly protected resource.

Conclusion

THIS ACTION IS MADE FINAL

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to 0 whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner, Art Unit 2183

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